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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,657	09/26/2001	Jari Melava	944-003.108	3087

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EXAMINER

CHANG, EDITH M

ART UNIT PAPER NUMBER

2637

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/965,657	Applicant(s) MELAVA, JARI	
	Examiner Edith M Chang	Art Unit 2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 26 September 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>20040301</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 2-6, 8, and 13 are objected to because of the following informalities:

Claims 2-4 & 8, line 1: "further comprising" is suggested changing to "wherein", since the prescaler of claim 1 does not further comprising other elements than the elements recited in the claim 1.

Claim 13, line 8: "signals" is suggested changing to "quadrature signals".

Claims 5-6 are dependent on the objected claim 3.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 2: "a ployphase filter having an input frequency signal" is not understood that a filter can have an input (or inputs) to receiving an input signal with an input frequency, but not has an input frequency signal; line 7: "its input" does not clearly indicate which input, the input of divider, the multiplexer or others; lines 11-12: "said output frequency signal is a desired fractional multiple of said input frequency signal" represents as the amplitude/magnitude of said

Art Unit: 2637

output frequency *signal* being a desired fractional multiple of said input frequency *signal*, and it does not clearly indicate the frequency of said output signal being a desired fractional multiple of said input signal regarding the invention.

Claim 4, line 4: “an output phase signal” does not clearly indicate that it is one of the “one or more output phase signals” recited in lines 2-3 of claim 1, or another output phase signal from somewhere.

Claim 9, lines 7, 7-8 & 11: “the selected phase signal”, “the phase signals”, and “the original selected phase” lack antecedent bases.

Claim 10, lines 1-2: “the phase signals” lacks antecedent basis.

Claims 2-3, 5-8, and 11-12 are directly or indirectly dependent on the rejected claims 1 and 9.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Craninckx et al. (“A 1,75-GHz/3-V Dual-Modulus Divide-by-128/129 Prescaler in 0.7- $\mu$ m CMOS” IEEE Journal of Solid-State Circuits, VOL. 31, NO. 7, July 1996, pages 890-897).

Regarding **claims 1, 9 & 13**, in Fig.1, Craninckx et al. teaches a PLL fractional-N

Art Unit: 2637

frequency synthesizer with a prescaler and in Fig.3, a dual modulus prescaler of the frequency synthesizer and its method, the prescaler comprises:

a M/S Half speed circuit/means (as the polyphase filter) receiving a signal on inputs F2 and  $\bar{F}2$  and outputting one or more phase signals having a phase difference 90 degree (Fig.3 F4.I, F4.Q,  $\bar{F}4.I$ ,  $\bar{F}4.Q$ , page 891, the right column, lines 4-8);

a Phase-select circuit/means (as a multiplexer) connected to the M/S Half speed circuit for selecting the one or more phase signals based on control signals C0, C1, and C2 (shown in Fig.7 C<sub>ctrl</sub> & on page 893, the right column, lines 6-7 & 15-17);

a /32 Low speed circuit/means (as an asynchronous divide-by-N block, page 891, the left column, the last 5 lines) connected to the Phase-select circuit to generate a Fout;

a Frequency Control circuit/means (as the phase control) generating the control signal C<sub>ctrl</sub> in response to C0, C1 and C2 (as the D-CTRL word signal), a Mode-input (as MOD signal), and a feedback signal outputted by the /32 Low speed circuit to the Phase-select circuit.

Regarding **claim 2**, Craninckx et al. teaches the low Mode-input disabling the Frequency Control (page 891, the left column, the last 7 & 6 lines).

Regarding **claim 3**, Craninckx et al. teaches the high Mode-input enabling the Frequency Control (page 891, the right column, the lines 3-4).

Regarding **claim 4**, in Fig.7, Craninckx et al. teaches the Phase-select selecting one of the multiple phase signals F4.I,  $\bar{F}4.I$ , F4.Q, and  $\bar{F}4.Q$  based on the values of C0, C1, and C2 (on page 893, the right column, lines 6-7 & 15-17).

Regarding **claims 5 & 6**, in Fig.7, Craninckx et al. teaches the division ration is  $N+C/4$ , where the value of C corresponds to the number of changes of the Frequency Control signal C<sub>ctrl</sub>

Art Unit: 2637

in one period, and the C is 4 (the 4 values are  $C_1 C_0$  &  $C_2 C_0$  which are 00, 01, 01, 11). Hence the division ration is  $N + 4/4 = N + 1$ , the divide-by-129 (page 891, the right column, lines 1-4).

Regarding **claim 7**, in Fig.3, Craninckx et al. teaches the Fin is a differential signal (page 891, the left column, the last paragraph, the lines 1-3).

Regarding **claims 8 & 10**, in page 891, the right column, lines 1-2, Craninckx et al. teaches that when the Mode-input is high, the Frequency Control block is enabled (selecting the phase signals outputted from the M/S Half speed block) and in turns the ratio of division increasing (such as from 128 to 129).

Regarding **claim 11**, in page 891, the right column, lines 14-16, Craninckx et al. teaches the dual-modulus operation of the prescaler.

Regarding **claim 12**, in Fig.3, Craninckx et al. teaches the Phase-select selecting four phases : F4.I/0 degree, F4.Q 90 degree,  $\overline{\text{F4.I}}$  180 degree, and  $\overline{\text{F4.Q}}$  270 degree.

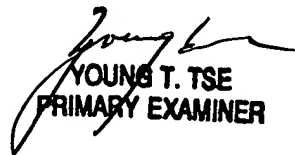
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2637

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang  
April 8, 2005



YOUNG T. TSE  
PRIMARY EXAMINER